

REMARKS

Claims 1-18 are pending. Claims 1 and 10 have been amended. Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

Entry of this Amendment is respectfully requested since no new issues are raised by entry of the Amendment and it places the application in condition for allowance.

Claim Rejections Under 35 U.S.C. § 103

Claims 1, 2, 4-11, and 13-18 were rejected under 35 U.S.C. § 103(a) over Applicants Admitted Prior Art (AAPA) in view of Nakao et al. (U.S. Patent No. 6,809,000); Claims 3 and 12 were rejected under 35 U.S.C. § 103(a) over AAPA and Nakao in view of Wolf et al. (Silicon Processing for the VLSI Era, Volume 1 – Process Technology, Second Edition, pages 216-219); claims 4, 7, 13, and 16 were rejected under 35 U.S.C. § 103(a) over AAPA and Nakao in view of Yasaitis et al. (EP 0472135 A1); claims 1, 2, 4-11, and 13-18 were rejected under 35 U.S.C. § 103(a) over AAPA in view of Kirlin et al. (U.S. Patent No. 6,320,213); claim 3 was rejected under 35 U.S.C. § 103(a) over AAPA and Kirlin in view of Wolf; and claims 4, 7, 13, and 16 were rejected under 35 U.S.C. § 103(a) over AAPA and Kirlin in view of Yasaitis. Applicants respectfully traverse these rejections.

Amended claim 1 recites, in part, a method for fabricating a capacitor that includes forming a second metal layer covering the patterned poly-silicon layer and first metal layer and the semiconductor substrate, wherein a side wall of the patterned first metal layer is electrically connected to the second metal layer.

As admitted in the Office Act, on pages 3 and 7, AAPA does not disclose a second metal layer as recited in claim 1. The Office Action relies on Nakao or Kirlin as allegedly teaching this feature. Nakao and Kirlin merely disclose diffusion layers for semiconductor devices. Neither of these references teach the structure recited in claim 1. Specifically, although the Office Action alleges that anti-diffusion film 17 in Nakao is analogous to the second metal layer recited in claim, the layer 17 is not configured such that a side wall of the patterned first metal layer is electrically connected to the second metal layer, as recited in claim 1. Similarly, the barrier layer 120 in Kirlin is not configured such that a side wall of the patterned first metal layer is electrically connected to the second metal layer, as recited in claim 1. Accordingly, no combination of AAPA, Nakao, and Kirlin teach or suggest, a method for fabricating a capacitor that includes forming a second metal layer covering the patterned poly-silicon layer and first metal layer and the semiconductor substrate, wherein a

side wall of the patterned first metal layer is electrically connected to the second metal layer, as recited in claim 1.

Claim 10 is believed allowable for at least the reasons presented above with respect to claim 1 since claim 5 similar features to those discussed above with respect to claim 1.

Claims 2-9 and 11-18 are believed allowable for at least the reasons present above with respect to claims 1 and 10 by virtue of their dependence upon claims 1 and 10 and because neither Wolf nor Yasaitis remedy at least the deficiencies of AAPA, Nakao, and Kirlin discussed above. Accordingly, Applicants respectfully request reconsideration and withdrawal of this rejection.

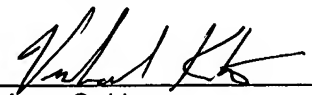
Conclusion

Therefore, all objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Should any issues remain unresolved, the Examiner is encouraged to contact the undersigned attorney for Applicants at the telephone number indicated below in order to expeditiously resolve any remaining issues.

Respectfully submitted,

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